REMARKS/ARGUMENT

Claims 1, 2, 4, 6-8 and 12 are amended. New claims 13 and 14 are added to more completely claim the invention. No new matter is added. Claims 1-14 are thus presented for prosecution.

Claims 1, 2 and 4-8 are rejected over Applicant's Admitted Prior Art ("APA") in view of U.S. Patent 3,980,959 to George ("George"). Claim 3 is rejected as being unpatentable over APA in view of George and further in view of U.S. Patent 5,982,781 to Przybyla et al. ("Przybyla") and U.S. Patent 5,570,306 to Soo ("Soo"). Claims 9 and 10 are rejected as being unpatentable over APA in view of George, and further in view of Przybyla. Claims 11 and 12 are rejected as being unpatentable over APA in view of George, Przybyla and Soo. Reconsideration of the application in light of the remarks below is respectfully requested.

Proposed new Figs. 1, 2 and 3 are enclosed with the changes indicated in red. Approval of these drawings is respectfully requested. Proposed formal Figs. 1-3 are also enclosed incorporating these changes.

Claims 1, 2 and 4-8 are rejected under 35 U.S.C. 103 as being unpatentable over APA in view of George.

In order to establish a prima facie case of obviousness, there must be shown: 1) a suggestion or motivation in the references or in the knowledge of one with ordinary skill in the art, to modify or combine the references 2) a reasonable expectation of success and 3) the prior art references must teach or suggest all of the claim limitations. M.P.E.P. §706.02(j). At least elements 1 and 3 are missing here.

Among the limitations of independent claims 1 and 2, which are neither shown nor suggested even in a combination of the art of record are:

> a capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus . . . .

Similarly, among the limitations of independent claim 7, which are neither shown nor suggested even in a combination of the art of record are:

> providing video data from a video processor to a plurality of paths independent of each other;
> sending said video data to a display through a frame buffer in at least one of said independent paths operating as a real time output path;
> sending said video data to a system memory through a system bus in at least another of said independent paths operating as a capture path; and

The Office Action states that these limitations are shown in APA. However, as is clearly shown in Fig. 3, and the corresponding text on pages 1 and 2 of the specification, the capturing path of APA shares at least frame buffer data bus 13 of the real time output path. Therefore, the capturing path is not "independent" of the real time output path as is claimed.

Moreover, there is no motivation shown for combining the gate of George with the structure disclosed in APA - as suggested in the Office Action. The Office Action merely states a perceived benefit of making the combination - that of producing a structure which would allow data to pass from the video processor to the system memory only when required. The Office Action must explain the reasons why one of ordinary skill in the art would be motivated to select the references or teachings and combine them. In re Rouffet, 47 U.S.P.Q.2d 1453, 1459 (Fed. Cir. 1998). A principle must be identified, known by those with ordinary skill in the art, that suggests the claimed invention. Id. Inventions are frequently the process of combining prior art in a nonobvious manner. Id. However, the Office Action is devoid of a motivation for actually making this combination. Without such a motivation, a prima facie case of obviousness cannot be made.

Therefore, it is asserted that independent claims 1, 2 and 7 are patentable over the art of record. Claims 4-6 and 8 include the above referenced limitations of independent claims 1 and 7 respectively, and include further limitations which, in combination with the limitations of claims 1 and 7, are also neither disclosed nor suggested in the art of record. It is asserted that these claims are patentable as well. For example, the Office Action does not set forth a prior art reference which shows a memory coupled to a gate as is claimed in claim 4. Moreover, the Office Action does not set forth a motivation for combining such a structure with the teachings of APA. Again, the Office

Action merely sets forth a perceived benefit of such a combination and does not show a motivation for making the combination.

Claim 3 is rejected as being obvious over APA in view of George and further in view of Przybyla and Soo. Claim 3 is dependent upon claim 2. As stated above, claim 2 includes limitations which are not shown even in a combination of APA in view of George. Przybyla and Soo are also devoid of such limitations. Therefore, it is asserted that claim 2 is patentable over Admitted Prior Art in view of George, Przybyla and Soo. Claim 3 is dependent upon 2 and includes further limitations which, in combination with the limitations of claim 2, are also neither disclosed nor suggested even in a combination the art of record.

Moreover, the Office Action merely cited what it asserts as being shown in the prior art and then indicates "it would have been obvious" to combine all of these teachings. However, the Office Action must explain the reasons why one of ordinary skill in the art would be motivated to select the references or teachings and combine them. In re Rouffet, 47 U.S.P.Q.2d 1453, 1459 (Fed. Cir. 1998). A principle must be identified, known by those with ordinary skill in the art, that suggests the claimed invention. Id. Inventions are frequently the process of combining prior art in a nonobvious manner. Id. However, the Office Action is devoid of a motivation for actually making the asserted combination. Without such a motivation, a prima facie case of obviousness cannot be made.

Claims 9 and 10 are rejected as being obvious over APA in view of George and further in view of Przybyla. Claims 9 and 10 are dependent upon claim 7. As stated above, claim 7 includes limitations which are not shown even in a combination of APA in view of George. Przybyla is also devoid of such limitations. Therefore, it is asserted that claim 7 is patentable over APA in view of Przybyla. Claims 9 and 10 are dependent upon claim 7 and includes further limitations which, in combination with the limitations of claim 7, are also neither disclosed nor suggested in the art of record. It is asserted that these claims are patentable as well.

Moreover, the Office Action merely cited what it asserts as being shown in the prior art and then indicates "it would have been obvious" to combine all of these teachings. However, the Office Action must explain the reasons why one of ordinary skill in the art would be motivated to select the references or teachings and combine them. In re Rouffet, 47 U.S.P.Q.2d 1453, 1459 (Fed. Cir. 1998). A principle must be identified, known by those with ordinary skill in the art, that suggests the

claimed invention. Id. Inventions are frequently the process of combining prior art in a nonobvious manner. Id. However, the Office Action is devoid of a motivation for actually making the asserted combination. Without such a motivation, a prima facie case of obviousness cannot be made.

Claims 11 and 12 are rejected as being obvious over APA in view of George and further in view of Przybyla and Soo. Claims 11 and 12 are dependent upon claim 7. As stated above, claim 7 includes limitations which are not shown even in a combination of APA in view of George. Przybyla and Soo are also devoid of such limitations. Therefore, it is asserted that claim 7 is patentable over APA in view of Przybyla and Soo. Claims 11 and 12 are dependent upon claim 7 and include further limitations which, in combination with the limitations of claim 7, are also neither disclosed nor suggested in the art of record. It is asserted that these claims are patentable as well.

Moreover, the Office Action merely cited what it asserts as being shown in the prior art and then indicates "it would have been obvious" to combine all of these teachings. However, the Office Action must explain the reasons why one of ordinary skill in the art would be motivated to select the references or teachings and combine them. In re Rouffet, 47 U.S.P.Q.2d 1453, 1459 (Fed. Cir. 1998). A principle must be identified, known by those with ordinary skill in the art, that suggests the claimed invention. Id. Inventions are frequently the process of combining prior art in a nonobvious manner. Id. However, the Office Action is devoid of a motivation for actually making the asserted combination. Without such a motivation, a prima facie case of obviousness cannot be made.

Reconsideration of the rejection of claims 1-12 under 35 U.S.C. § 103 is respectfully requested in light of the remarks above.

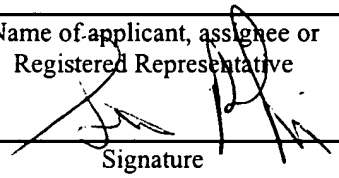
Applicant has responded to all of the rejections and objections recited in the Office Action and Notice of Allowance for all of the pending claims is therefore respectfully requested.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on January 11, 2002:

Steven S. Rubin

Name of applicant, assignee or Registered Representative



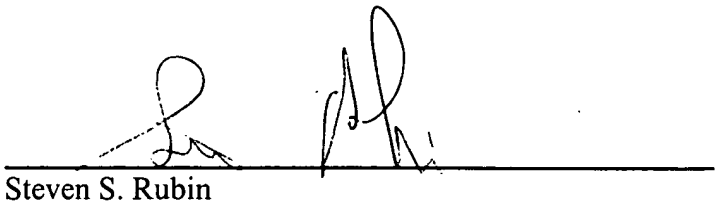
Signature

January 11, 2002

Date of Signature

SIW/SSR:swu:dmk:mcm

Respectfully submitted,



Steven S. Rubin
Registration No.: 43,063
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph at page 1, line 8:

FIG. 3 is a block diagram showing an example of a conventional video data transfer system. As shown in the figure, video data decoded by a video decoder 11 is sent via a video port 12 to a graphic accelerator 30 having [the] a video input function. Upon receiving video data, the graphic accelerator 30, which comprises a video processor 21, display control circuit 22, and a FIFO memory 24, causes the video processor 21 to perform predetermined signal processing for the received video data and outputs the processed video data to a frame buffer 14 via a frame buffer data bus 13 for storage in an internal off-screen memory 15.

Paragraph at page 2, line 22:

The present invention seeks to solve the problems associated with the prior art described above. It is an object of the present invention [is] to provide a video data transfer system which increases the capturing rate of video data to be sent to the system memory.

Paragraph at page 4, line 5:

An embodiment of the present invention is described with reference to the attached drawings. FIG. 1 is a block diagram of the embodiment of the video data transfer system according to the present invention. As shown in FIG. 1, a video decoder 11 is connected via a video port 12 to a graphic accelerator 20 which has [the] a video input function. This graphic accelerator 20 is connected to a frame buffer 14 via a frame buffer data bus 13, to a system memory 18 via a system bus 17, and to a display 16. The graphic accelerator 20 has a video processor 21, a display control circuit 22, a gate 23, and a FIFO memory 24.

Paragraph beginning at page 6, line 24:

The configuration of the embodiment according to the present invention is detailed with reference to FIG. 1. The graphic accelerator 20 with [the] a video input function is implemented as a

large scale integrated circuit (LSI). It comprises the video processor 21 which reduces the size of video data according to the YUV 16 bits, the real time output path 25 which is a 64-bit internal bus through which video data from the video processor 21 is sent to the display control circuit 22 via the frame buffer 14, and the capturing-only path 26 which is a 32-bit internal bus through which video data from the video processor 21 is sent to the FIFO memory 24 via the gate 23.

CLAIMS:

1. A video data transfer system comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a [capturing-only] capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus; and

a gate in said [capturing-only] capturing path, said gate being controllable to permit said video data to pass when received from said video processor.

2. A video data transfer system, comprising:

a real time output path through which video data processed by a video processor is sent to a display via a frame buffer;

a [capturing-only] capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus, wherein

said real time output path comprises:

an off-screen memory which receives video data from said video processor via a data bus and stores video data therein, said off-screen memory being in the frame buffer; and

a display control circuit which receives video data read from said off-screen memory via said data bus for enlargement and interpolation processing and transfers processed results to said display, and wherein

said [capturing-only] capturing path comprises:

a gate which is opened only when video data is received from said video processor for capturing; and

memory means for storing said video data sent through said gate and for transferring said video data to said system bus.

4. A video data transfer system as defined in claim 1, further comprising:

a capture path memory in said [capturing-only] capturing path;

said capture path memory being connected to said gate; and

said capture path memory being operable to store said video data passed by said gate.

6. A video data transfer system as defined in claim 5, wherein said real time output path further comprises:

an off-screen memory effective to receive said video data from said video processor via a data bus and [stores] store said video data therein; and wherein

said off-screen memory [being] is in said frame buffer.

7. A video data transfer method, comprising:

providing video data from a video processor to a plurality of paths independent of each other;

sending said video data to a display through a frame buffer in at least one of said independent paths operating as a real time output path;

sending said video data to a system memory through a system bus in at least another of said independent paths operating as a [capture-only] capture path; and

controlling said [capture-only] capture path to permit said video data to pass to said system memory when said video data is to be captured.

8. A video data transfer method as defined in claim 7, further comprising storing said video data in a capture path memory in said [capture-only] capture path when said video data is permitted to pass to said system memory.

12. A video data transfer method as defined in claim 11, further comprising controlling said [capture-only] capture path to prevent said video data from being stored in said capture path memory when said capture path memory contains said at least one of a field and a frame delimiter.